In the specification:

Please replace paragraphs [0005], [0019], and [0021] with the following replacement paragraphs:

[0005] One popular IO bus is the Peripheral Component Interconnect (PCI), used in many personal computers (PCs), computer servers, storage and network systems. The PCI bus can connect to a wide variety of devices, including memory, disk drives, graphics systems, and controllers to other buses, such as Universal-Serial-Bus (USB) and FireWire (IEEE 1394). A ~~wide variety input-output~~ wide variety of input-output devices can be accessed through these other buses, such as memory cards, pointing devices (mice), music devices, printers, etc. The types of bus accesses for this wide variety of devices is quite varied. Predicting ahead in such a varied environment is challenging, yet a good prediction scheme could improve bus performance.

[0019] Since a PC user ~~may desired to~~ may desire to install many peripheral devices or PCI add-on cards to the PC, a second PCI bus is useful. Secondary PCI bus 22 can be larger, or have more available connections, than primary PCI bus 20, allowing for more devices 24 to be installed. PCI devices 24 do not add load to primary PCI bus 20 since PCI-to-PCI bridge 18 buffers the physical lines of secondary PCI bus 22 from the lines of primary PCI bus 20.

[0021] PCI-to-PCI bridge 18 contains cache buffer 82, which can store pre-fetched data for the current read command. For example, when CPU 10 reads a memory block on one of devices 24, prefetch controller 62 in PCI-to-PCI bridge 18 may fetch ahead when reading the memory block on device 24. The pre-fetched data is then available for satisfying the current read command if it continues to accept ~~data over and extended~~ data over an extended burst. The additional data read from device 24 is stored in cache buffer 82. If CPU 10 extends the current cycle with a longer burst access, then the additional data can be sent directly from cache buffer 82 over primary PCI bus 20 to CPU 10 without ~~performing a another~~ performing another read transaction of device 24 over secondary PCI bus 22.